

FEATURES

- 15pF HCMOS/ TTL logic
- Tri-State enable/disable
- Wide frequency range
- Resistance weld package
- 3.3V operation (optional)

CLOCK OSCILLATOR

The THSCR Series clock oscillator can drive both HCMOS and TTL logic. This oscillator also features tri-state enable/disable capabilities in a 14 pin DIP package.

PART NUMBERING GUIDE "EXAMPLE"

PART NUMBER *	FREQUENCY STABILITY
THSCR2	±100 PPM
THSCR1	±50 PPM
THSCR0	±25 PPM

* Complete part number to include frequency. i.e. THSCR2-10.000MHz

OPERATING CONDITIONS/ELECTRICAL CHARACTERISTICS

PARAMETERS	FREQUENCY RANGE	CONDITIONS	MINIMUM	TYPICAL	MAXIMUM	UNITS
FREQUENCY RANGE (f_0)	1.000 ~ 100.000		1.000		100.000	MHz
OPERATING TEMP. RANGE (T_{OPR})	1.000 ~ 100.000		0		+70	°C
STORAGE TEMP. RANGE (T_{STG})	1.000 ~ 100.000		-55		+125	°C
FREQUENCY STABILITY	1.000 ~ 100.000	All conditions*	-100		+100	PPM
INPUT CURRENT (I_{DD})	1.000 ~ 25.000			17	25	mA
	25.000 ~ 50.000			33	40	mA
	50.000 ~ 80.000			45	77	mA
	80.000 ~ 100.000			67	82	mA
OUTPUT SYMMETRY	1.000 ~ 100.000	50% V_{DD} level	40	50 ±3	60	%
						%
RISE TIME (T_R)	1.000 ~ 100.000	10% ~ 90% V_{DD} level			5	nS
FALL TIME (T_F)	1.000 ~ 100.000	90% ~ 10% V_{DD} level			5	nS
OUTPUT VOLTAGE (V_{OL}) (V_{OH})	1.000 ~ 100.000	$I_{OL} = 16$ mA	4.5		0.5	V
						$I_{OH} = -16$ mA
OUTPUT CURRENT (I_{OL}) (I_{OH})	1.000 ~ 100.000	$V_{OL} = 0.5$ V			16	mA
						$V_{OH} = 4.5$ V
OUTPUT LOAD	1.000 ~ 100.000	TTL			10	TTL
						15
START-UP TIME (T_s)	1.000 ~ 100.000				10	mS
SUPPLY VOLTAGE		+5.0 ±0.25				V

* Inclusive of 25°C tolerance, operating temperature range, input voltage change, load change, aging, shock and vibration.

** An internal pullup resistor from pin 1 to pin 14 allows active output if pin 1 is left open.

PACKAGE DIMENSIONS (mm)

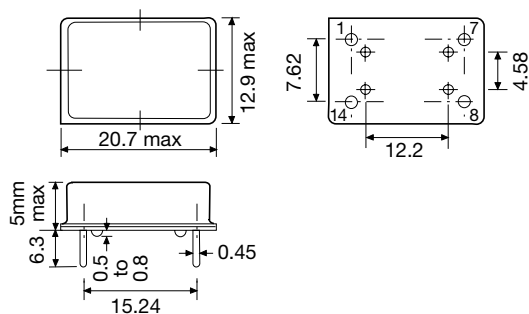


Figure 1) THSCR Series – Top, Bottom and Side views

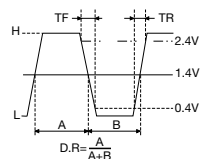


Figure 2) TTL Output Wave Form

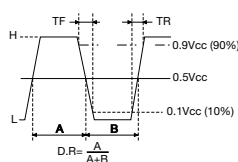


Figure 3) HCMOS Output Wave Form

PIN CONNECTIONS

#1	TRI-STATE
#7	CASE GROUND
#8	OUTPUT
#14	+5V DC

ENABLE / DISABLE FUNCTION**

INH (PIN 1)	OUTPUT (PIN 8)
OPEN**	ACTIVE
1 LEVEL $V_{IH} \geq 2.2$ V ($V_{IH} \geq 2.0$ V ABOVE 70MHz)	ACTIVE
'0' LEVEL $V_{IL} \leq 0.8$ V	HIGH Z