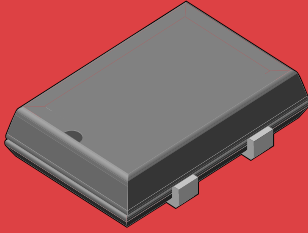


## FEATURES

- Extended temperature range capabilities
- Optional 3.3V available from 1.000 ~ 30.000MHz
- Tri-State enable/disable
- Tape and Reel (1,000 pcs)



## SMD CLOCK OSCILLATOR

The SMJ Series oscillator is compatible with both TTL and HCMOS technologies. The J-leaded configuration and high resistance to soldering temperature makes it ideal for surface mount production processes. The SMJ offers low power consumption of HCMOS, but will also drive full 10 TTL gates when used in a TTL application.

## PART NUMBERING GUIDE \*EXAMPLE\*

PART NUMBER*	SUPPLY VOLTAGE	PART NUMBER*	SUPPLY VOLTAGE
SMJ THSC2	5.0 ±0.5V	SMJ HSC2	5.0 ±0.5V
SMJ T2	5.0 ±0.5V		

\* Complete part number to include frequency i.e. SMJ THSC2-16.000MHz

## OPERATING CONDITIONS/ELECTRICAL CHARACTERISTICS

PARAMETERS	CONDITIONS	SMJ THSC2		SMJ T2		SMJ HSC2		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
FREQUENCY RANGE	$f_0$	1.000	50.000	1.000	70	1.0	70	MHz
FREQUENCY STABILITY	-10 ~ +70°C*	-100	+100	-100	+100	-100	+100	PPM
	-40 ~ +85°C*	-200	+200	-200	+200	—	—	PPM
INPUT CURRENT ( $I_{DD}$ )	No Load		23		35		35	mA
	Output Disabled ( $I_z$ )		12		25		20	mA
OUTPUT SYMM. (CMOS)	(Vdd/2)	40	60	—	—	40	60	%
	(TTL) (1.4V)	40	60	40	60	—	—	%
RISE TIME ( $T_r$ )	20% ~ 80% Vdd		8		5		7	nS
	0.4V ~ 2.4V		8		5		7	nS
FALL TIME ( $T_f$ )	80% ~ 20% VDD		8		5		7	nS
	2.4V ~ 0.4V		8		5		7	nS
OUTPUT VOLTAGE ( $V_{OL}$ )	$I_{OL} = \text{max.}$		0.4		0.4		0.4	V
	$I_{OH} = \text{max.}$	Vdd -0.4		2.4		Vdd -0.4		V
OUTPUT CURRENT ( $I_{OL}$ )	$V_{OL} = \text{max.}$		16		16		4.0	mA
	$V_{OH} = \text{min.}$		-0.4		-0.4		-4.0	mA
OUTPUT LOAD	HCMOS		50				50	pF
	TTL		10		10			TTL
START-UP TIME ( $T_s$ )			4		10		10	mS
OUTPUT ENABLE/DISABLE TIME			100		100		100	ns
LOGIC		TTL/CMOS		TTL		CMOS		
STOR. TEMP. RANGE ( $T_{STG}$ )	-55 ~ +125°C							°C
SUPPLY VOLTAGE ( $V_{DD}$ )		5.0 ±0.5V		5.0 ±0.5V		5.0 ±0.5V		VDD

\* Inclusive of 25°C tolerance, operating temperature range, input voltage change, load change, aging shock and vibration.

\*\* An internal pullup resistor from pin 1 to 14 allows active output if pin 1 is left open.

## PACKAGE DIMENSIONS (mm)

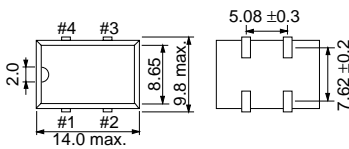


Figure 1) SMJ Top and Side view

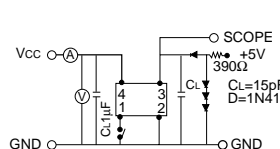


Figure 2) TTL Measurement Circuit

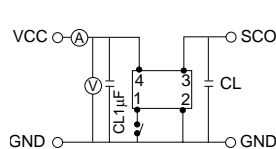


Figure 3) CMOS Measurement Circuit

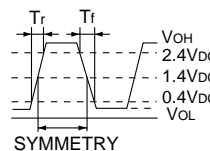


Figure 4) TTL Output Waveform

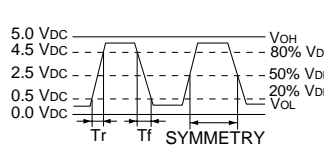


Figure 5) CMOS Output Waveform

PIN CONNECTIONS	
#1	ENABLE/DISABLE**
#2	GND
#3	OUT
#4	VDD

ENABLE / DISABLE FUNCTION** 5.0 ± 0.5V	
INH (Pin 1)	OUTPUT (Pin 3)
OPEN**	ACTIVE
*1* Level VIH ≥ 2.0V (SMJHSC2, SMJTHSC2)	ACTIVE
*1* Level VIH ≥ 3.5V (SMJ T2)	ACTIVE
*0* Level VIL ≤ 0.8V (SMJHSC2, SMJTHSC2)	High Z
*0* Level VIL ≤ 1.5V (SMJHSC2, SMJTHSC2)	High Z

\*\* An internal pullup resistor from pin 1 to pin 14 allows active output if pin 1 is left open.